



Docket No.: M4065.0335/P335-A  
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:  
Howard E. Rhodes

Application No.: 09/318,159

Group Art Unit: 2811

Filed: May 25, 1999

Examiner: G. Munson

For: TRENCH ISOLATION FOR  
SEMICONDUCTOR DEVICES

*Handwritten:* #29/1000  
*Signature:* [illegible]  
*Date:* 10/00

RECEIVED  
SEP 10 2002  
TECHNOLOGY CENTER 2800

AMENDMENT

Box Non-Fee Amendment  
Commissioner for Patents  
Washington, DC 20231

Dear Sir:

Prior to examination on the merits, please amend the above-identified U.S. patent application as follows:

In the Claims:

Please cancel claims 49, 57, 71, 72, 75 and 76.

Please rewrite claims 45, 50-52, 68, 70 and 73 as shown in the Replacement Claims.

Please add the following new claim:

77. (New) An integrated circuit comprising:

a semiconductor substrate including a first region of a predefined conductivity type;

*Handwritten:* De  
*Handwritten:* subject

56 a field isolation region for separating said first region into at least two active regions, wherein said field isolation region includes an isolation trench, said isolation trench further including a first dielectric material forming sidewalls of said isolation trench and provided on a bottom of said isolation trench, and a second dielectric material situated within said sidewalls and provided over said first dielectric material, said first dielectric material being different than said second dielectric material;

at least a portion of a memory cell provided in at least one of said two active regions; and

a doped region formed within said first region and below said isolation trench, said doped region being of said predefined conductivity type and having a doping concentration higher than a doping concentration of said first region, wherein additional dopants in said doped region causing said higher dopant concentration are displaced away from said separated active regions.